WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells which are slower in a write operation than in a read operation; and

a cache memory for mediating an access to said plurality of memory banks from the outside,

said cache memory having a number of way equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells.

2. A semiconductor device according to claim 1, wherein:

said cache memory has a plurality of sets corresponding to the number of ways, and

each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks.

3. A semiconductor device according to claim 1, wherein:

when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory.

4. A semiconductor device according to claim 1, wherein:

when first data is written into said semiconductor device from the outside, wherein said

cache memory does not hold an address at which said first data is to be written, data held in an associated entry of said cache memory is written back to one of said plurality of memory banks, and said first data is written into said cache memory.

5. A semiconductor device according to claim 4, wherein:

when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside, the data is written back to a second memory bank included in said plurality of memory banks.

6. A semiconductor device according to claim 1, further comprising a plurality of data input/output nodes for inputting/outputting data to/from the outside,

wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device.

7. A semiconductor device according to claim 1, further comprising:

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line

comprised of a plurality of sublines, and

$$A = N \cdot B$$

is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus.

8. A semiconductor device according to claim 7, wherein:

said cache memory has a plurality of flags each associated with one subline for managing data held thereon; and

when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank.

9. A semiconductor device according to claim 7, wherein:

when said flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory.

10. A semiconductor device according to claim 1, wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or an phase change memory cell.

11. A semiconductor device according to claim 10, wherein said cache memory comprises SRAM memory cells.

12. A semiconductor device according to claim 1, wherein said cache memory comprises SRAM memory cells.

13. A semiconductor device comprising:

a plurality of memory banks, each having a

plurality of memory cells; and

a cache memory for communicating a write data to said plurality of memory banks,

wherein said semiconductor device performs a destructive read operation to read data from said memory cells.

14. A semiconductor device according to claim 13, wherein each said memory cell is a ferroelectric memory cell.

15. A semiconductor device according to claim 13, wherein:

when a write cycle of said memory cells is longer than a cycle of said destructive read operation, said cache memory has a degree of association larger than a value (m/n) determined by a ratio of a write cycle of said memory cells to a destructive read cycle (n) of said memory cell.

16. A semiconductor device according to claim 15, wherein:

said cache memory has at least two or more degree of association, i.e., a set size equal to or larger than two, and

one set has a capacity equal to or larger than the capacity of one said memory bank.

17. A semiconductor device according to claim 13, wherein said cache memory comprises SRAM memory cells.

18. A semiconductor device comprising:

a plurality of memory banks, each having a

plurality of memory cells; and

a cache memory for communicating a write data to said plurality of memory banks,

wherein said memory cells include either SESO (Single Electron Shut Off) memory cells or phase change memory cells, and

said cache memory has a degree of association equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells.

19. A semiconductor device according to claim 18, wherein:

said cache memory comprises SRAM memory cells.